Claims

1. A semiconductor device with a plurality of bonding pads each having a first metal formed using a top layer wiring layer, and a plurality of second metals each of which has a line shape, is arranged under the first metal, and is connected with the first metal concerned, wherein

the bonding pads are put in order and located to a long-side direction of the second metal which has a line shape.

2. A semiconductor device according to claim 1, wherein

width W and interval D in a bottom of the second metals satisfy a relation: $W \leqq D \leqq 2 \times W$.

3. A semiconductor device according to claim 1, wherein

the second metals are embedded in an insulating layer under the first metal, and an upper part is connected mutually in the insulating layer concerned.

4. A semiconductor device according to claim 1, further comprising:

a first lower-layer wiring layer of one layer under than the top layer wiring layer;

wherein the bonding pad further has a third metal which is arranged under the second metal, connected with the second metal concerned, and formed using the first lower-layer wiring layer.

5. A semiconductor device according to claim 1, further comprising:

a first lower-layer wiring layer of one layer under than the top layer wiring layer;

wherein the bonding pad further has an etching stopper which is arranged under the second metal and formed using a barrier metal of the first lower-layer wiring layer front surface.

6. A semiconductor device according to claim 1, further comprising:

a second lower-layer wiring layer below the bonding pad; and

a plurality of fourth metals of predetermined shape which are arranged over a wiring by the second lower-layer wiring layer in a region of a lower part of the bonding pad, and are connected to the wiring concerned.

7. A semiconductor device according to claim 6, wherein

in a region of a lower part of the bonding pad, the wiring by the second lower-layer wiring layer is divided into a shape of a plurality of lines.

8. A semiconductor device according to claim 1, further comprising:

a second lower-layer wiring layer below the bonding pad;

wherein in a region of a lower part of the bonding pad, a wiring by the second lower-layer wiring layer is divided into a shape of a plurality of lines.

9. A semiconductor device with a bonding pad having a first metal formed using a top layer wiring layer, and a plurality of second metals each of which has a line shape, is arranged under the first metal, and is connected with the first metal concerned, wherein

the second metals are embedded in an insulating layer under the first metal, and an upper part is connected mutually in the insulating layer concerned.

10. A semiconductor device according to claim 9, wherein

width W and interval D in a bottom of the second metals satisfy a relation: $W \leqq D \leqq 2 \times W$.

11. A semiconductor device according to claim 9, further comprising:

a first lower-layer wiring layer of one layer under than the top layer

wiring layer;

wherein the bonding pad further has a third metal which is arranged under the second metal, connected with the second metal concerned, and formed using the first lower-layer wiring layer.

12. A semiconductor device according to claim 9, further comprising:

a first lower-layer wiring layer of one layer under than the top layer wiring layer;

wherein the bonding pad further has an etching stopper which is arranged under the second metal and formed using a barrier metal of the first lower-layer wiring layer front surface.

13. A semiconductor device according to claim 9, further comprising:

a second lower-layer wiring layer below the bonding pad; and

a plurality of fourth metals of predetermined shape which are arranged over a wiring by the second lower-layer wiring layer in a region of a lower part of the bonding pad, and are connected to the wiring concerned.

14. A semiconductor device according to claim 13, wherein

the wiring by the second lower-layer wiring layer in a region of a lower part of the bonding pad is divided into a shape of a plurality of lines.

15. A semiconductor device according to claim 9, further comprising:

a second lower-layer wiring layer below the bonding pad;

wherein in a region of a lower part of the bonding pad, a wiring by the second lower-layer wiring layer is divided into a shape of a plurality of lines.

16. A semiconductor device with a bonding pad having a first metal formed using a top layer wiring layer, and a plurality of second metals each of which has a line shape, is arranged under the first metal, and is connected

with the first metal concerned,

wherein

the semiconductor device concerned has a first lower-layer wiring layer of one layer under than the top layer wiring layer; and

the bonding pad has an etching stopper which is arranged under the second metal and formed using a barrier metal of the first lower-layer wiring layer front surface.

17. A semiconductor device according to claim 16, wherein

width W and interval D in a bottom of the second metals satisfy a relation: $W \leqq D \leqq 2 \times W$.

18. A semiconductor device according to claim 16, further comprising:

a second lower-layer wiring layer below the bonding pad; and

a plurality of fourth metals of predetermined shape which are arranged over a wiring by the second lower-layer wiring layer in a region of a lower part of the bonding pad, and are connected to the wiring concerned.

19. A semiconductor device according to claim 18, wherein

in a region of a lower part of the bonding pad, the wiring by the second lower-layer wiring layer is divided into a shape of a plurality of lines.

20. A semiconductor device according to claim 16, further comprising:

a second lower-layer wiring layer below the bonding pad;

wherein in a region of a lower part of the bonding pad, a wiring by the second lower-layer wiring layer is divided into a shape of a plurality of lines.

21. A semiconductor device, comprising:

a bonding pad;

a wiring which passes along a lower part of the bonding pad; and

a plurality of metals of predetermined shape over the wiring in a region of a lower part of the bonding pad.

22. A semiconductor device according to claim 21, wherein

in a region of a lower part of the bonding pad, the wiring is divided into a shape of a plurality of lines.

23 A semiconductor device, comprising:

a bonding pad;

an output buffer which outputs a signal to the bonding pad;

an input buffer into which a signal applied to the bonding pad is inputted; and

an internal circuit connected to an input side of the output buffer, and to an output side of the input buffer;

wherein the bonding pad is formed above the output buffer, and is not formed above the input buffer and the internal circuit.

24. A semiconductor device according to claim 23, wherein

the output buffer includes a PMOS transistor and an NMOS transistor; and

the bonding pad is formed above one transistor among the PMOS transistor and the NMOS transistor, and is not formed above the other transistor.

25. A semiconductor device according to claim 24, wherein

the one transistor is the PMOS transistor, and the other transistor is the NMOS transistor.

26. A semiconductor device according to claim 24, wherein

the bonding pad, a drain of the PMOS transistor, and a drain of the NMOS transistor are electrically connected to a common wiring, and in the

common wiring, a connecting part to the bonding pad is between a connecting part to the drain of the PMOS transistor, and a connecting part to the drain of the NMOS transistor.

27. A semiconductor device according to claim 23, wherein

the output buffer includes a PMOS transistor and an NMOS transistor, and the bonding pad is formed ranging over an upper part of the PMOS transistor and the NMOS transistor of the output buffer.

28. A semiconductor device according to claim 23, wherein

the bonding pad has a first metal formed using a top layer wiring layer, and a plurality of second metals each of which has a line shape, is arranged under the first metal, and is connected with the first metal concerned.

29. A semiconductor device according to claim 28, further comprising:

a plurality of the bonding pads;

wherein the bonding pads are arranged and located to a long-side direction of the second metal having a line shape.

30. A semiconductor device according to claim 28, wherein

width W and interval D in a bottom of the second metals satisfy a relation: $W \leqq D \leqq 2 \times W$.

31. A semiconductor device according to claim 23, wherein

a wiring divided into a shape of a plurality of lines is formed in a region of a lower part of the bonding pad.

32. A semiconductor device, comprising:

a bonding pad;

an output buffer which outputs a signal to the bonding pad;

an input buffer into which a signal applied to the bonding pad is inputted; and

an internal circuit connected to an input side of the output buffer, and an output side of the input buffer;

wherein the bonding pad is formed ranging over an upper part of the output buffer and the input buffer, and an upper part of a part of the internal circuit.

33. A semiconductor device according to claim 32, wherein

the bonding pad includes a first metal formed using a top layer wiring layer, and a plurality of second metals each of which has a line shape, is arranged under the first metal, and is connected with the first metal concerned.

34. A semiconductor device according to claim 33, further comprising:

a plurality of the bonding pads;

wherein the bonding pads are arranged and located to a long-side direction of the second metal having a line shape.

35. A semiconductor device according to claim 33, wherein

width W and interval D in a bottom of the second metals satisfy a relation: $W \leqq D \leqq 2 \times W$.

36. A semiconductor device according to claim 32, wherein

a plurality of wirings divided into a shape of a line are formed in a region of a lower part of the bonding pad.